CLAIMED INVENTION

What is claimed is:

1. A method comprising:

monitoring processor utilization of a computer system having a processor, the processor having a plurality of performance levels; and

automatically transitioning the processor to a higher performance level if it is determined that the processor utilization has remained above a switch-up level for a specified time.

2. The method of claim 1, wherein the number of performance levels is two.

3. The method of claim 1, wherein the switch-up level is approximately 95% of a current processor performance level.

4. The method of claim 1, further comprising:

automatically transitioning the processor to a next lower performance level, if any, if it is determined that the processor utilization has remained below a switch-down level for a specified time.

5. The method of claim 4, wherein the switch-down level is approximately 95% of the next lower processor performance level.

6. An apparatus comprising:

a processor;

a first input node to receive a first signal, the first signal indicating that processor utilization has exceeded a first threshold for a first period of time such that the processor is transitioned to a higher performance level in response to the first signal; and

a second input node to receive a second signal, the second signal indicating

that processor utilization has fallen below a second threshold for a second period of time such that the processor is transitioned to a lower performance level in response to the second signal.

7. The apparatus of claim 6, wherein the first threshold is approximately 95% of a current processor performance level.

8. The apparatus of claim 6, wherein the first period of time is equal to the second period of time.

9. A machine-readable medium that provides executable instructions, which when executed by a processing system, cause said processing system to perform a method, the method comprising:

periodically monitoring processor utilization of a computer system having a processor, the processor having a plurality of performance levels; and

automatically transitioning the processor to a higher performance level if it is determined that the processor utilization has remained above a switch-up level for a specified time.

10. The machine-readable medium of claim 9, wherein the number of performance levels is two.

11. The machine-readable medium of claim 9, wherein the switch-up level is approximately 95% of a current processor performance level.

12. The machine-readable medium of claim 9, further comprising:

automatically transitioning the processor to a next lower performance level,

if any, when the processor utilization has remained below a switch-down level for a specified period of time.

13. The machine-readable medium of claim 12 wherein the specified period of time that the processor utilization has remained above a switch-up level to transition the processor to a higher performance level is different than the specified period of time that the processor utilization has remained below a switch-down level to transition the processor to a next lower performance level.

14. The machine-readable medium of claim 12, wherein the switch-down level is approximately 95% of the next lower processor performance level.

15. The machine-readable medium of claim 12, wherein the specified period of time that the processor utilization has remained above a switch-up level to transition the processor to a higher performance level is greater than a processor-utilization monitoring periods.

16. The machine-readable medium of claim 15, wherein the specified period of time that the processor utilization has remained below a switch-down level to transition the processor to a next lower performance level equal to the processor-utilization monitoring period.